Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Please amend the claims as follows:

1– 88. (Cancelled)

89. (Currently Amended) A processor comprising:

first logic to detect an error;

second logic to attempt to correct a detected error; and

a first interface to a first memory external to the processor that stores a set of procedures to access the processor across different processor implementations and at least a first software error handling routine to be invoked by the processor via the first interface when the second logic cannot correct the detected error.

90. (Previously presented) The processor of claim 89, wherein the first memory further stores a second software error handling routine to be invoked by the processor when the first software error handling routine cannot correct the detected error.

91. (Currently Amended) The processor of claim 90, further comprising:

a second interface to a second memory that stores an operating system, wherein the operating system includes a third software error handling routine to be invoked by the ~~processor~~ CPU when the second software error handling routine cannot correct the detected error.

92. (Previously presented) The processor of claim 90, wherein the first interface couples to a second memory that stores an operating system, wherein the operating system

includes a third software error handling routine to be invoked by the processor when the second software error handling routine cannot correct the detected error.

93. (Previously presented) A system comprising:

a processor;

a first memory coupled to the processor, the first memory to store at least a first firmware error handling routine to be invoked by the processor to attempt to correct a detected error when the processor cannot correct the detected error; and

a display coupled to the processor.

94. (Previously presented) The system of claim 93, wherein the first firmware error handling routine is to save a status of the detected error and at least a portion of the processor's state information.

95. (Previously presented) The system of claim 94, wherein the first memory further to store a second firmware error handling routine to be invoked by the processor to attempt to correct the detected error when the first firmware error handling routine cannot correct the detected error.

96. (Previously presented) The system of claim 94, wherein the second firmware error handing routine to determine the severity of the detected error by analyzing the processor's saved state information and the detected error, and to save additional state information.

97. (Previously presented) The system of claim 93, wherein the first memory further to store a second firmware error handling routine to be invoked by the processor after the first firmware error handling routine has been invoked.

98. (Previously presented) The system of claim 94, further comprising:

a second memory coupled to the processor, the second memory to store an operating system that includes a third error handling routine that is invoked by the processor to attempt to correct the detected error when the first and second firmware error handling routines cannot correct the detected error.

99. (Previously presented) The system of claim 98, wherein the processor is reset if the detected error cannot be corrected by the third error handling routine.

100. (Previously presented) The system of claim 99, wherein the processor is to detect the detected error.

101. (Previously presented) A system comprising:

a non-volatile memory to store firmware including a processor abstraction layer (PAL) and a system abstraction layer (SAL), wherein the PAL provides an interface to access the processor across different processor implementations and a first error handling routine and the SAL isolates an operating system from implementation differences in the system and provides a second error handling routine to be invoked if the first error handling routine cannot correct a detected error; and

a processor coupled to the non-volatile memory, the processor to execute the first and second error handling routines to attempt to correct an error.

102. (Previously presented) The system of claim 101, wherein the first error handling routine to save a status of the error and at least a portion of state information associated with the error.

103. (Previously presented) The system of claim 102, wherein the second error handing routine to determine the severity of the detected error by analyzing the saved state information and the error, and to save additional state information.

104. (Previously presented) The system of claim 103, further comprising:

a second memory coupled to the processor, the second memory to store an operating system that includes a third error handling routine that is invoked by the processor to attempt to correct the error when the first and second error handling routines cannot correct the detected error.

105. (New) A processor comprising:

first logic to detect an error;

second logic to attempt to correct a detected error; and

a first external interface to a first memory that stores at least a first software error handling routine to be invoked by the processor via the first interface when the second logic cannot correct the detected error and a second software error handling routine to be invoked by the processor when the first software error handling routine cannot correct the detected error.

106. (New) The processor of claim 89, wherein the second logic is adapted to correct a single bit error correcting code (ECC) error.

107. (New) The processor of claim 89, wherein the processor is to signal the memory with a correctable machine check (CMC) signal to inform the memory that an error has occurred and been corrected when the second logic corrects a detected error.

108. (New) The processor of claim 89, wherein upon the first logic detecting an error generates a machine check abort (MCA) to indicate that a hardware error or error has occurred.

109. (New) The processor of claim 89, wherein the first software error handling routine to:

determine if the detected error is processor related;

save minimal state information; and

attempt to correct the detected error.